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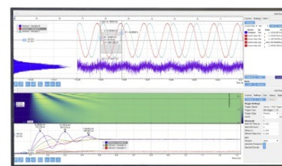

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Multifunctional tunneling devices based on graphene/*h*-BN/$MoSe_2$ van der Waals heterostructures

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The vertically stacked devices based on van der Waals heterostructures (vdWHs) of two-dimensional layered materials (2DLMs) have attracted considerable attention due to their superb properties. As a typical structure, graphene/hexagonal boron nitride (*h*-BN)/graphene vdWH has been proved possible to make tunneling devices. Compared with graphene, transition metal dichalcogenides possess intrinsic bandgap, leading to high performance of electronic devices. Here, tunneling devices based on graphene/*h*-BN/$MoSe_2$ vdWHs are designed for multiple functions. On the one hand, the device shows a typical tunneling field-effect transistor behavior. A high on/off ratio of tunneling current (5×10^3) and an ultrahigh current rectification ratio (7×10^5) are achieved, which are attributed to relatively small electronic affinity of $MoSe_2$ and optimized thickness of *h*-BN. On the other hand, the same structure also realizes 2D non-volatile memory with a high program/erase current ratio ($>10^5$), large memory window (~150 V from ±90 V), and good retention characteristic. These results could enhance the fundamental understanding of tunneling behavior in vdWHs and contribute to the design of ultrathin rectifiers and memory based on 2DLMs. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4982691]

Owing to their promising potentials in the next generation of electronic and optoelectronic devices, two-dimensional layered materials (2DLMs), including graphene (Gr), hexagonal boron nitride (*h*-BN), transition metal dichalcogenides (TMDs), etc., have triggered worldwide interest.[1–4] The van der Waals heterostructures (vdWHs) assembled from these families endow not only a possibility of preparing artificial materials with desired properties but also a platform for constructing multi-functional devices because of their atomically flat heterointerface and superior properties.[4–8] In a typical vdWH, a barrier-layer sandwiched tunneling structure is well acknowledged for exhibiting good performance in rectifiers,[9,10] memories,[11–13] light-emitting diodes,[14] and photodetectors.[15] Aiming at constructing such a structure, Gr has been frequently used as one of the components being electrons/holes provider due to its Fermi level tunability and ultrahigh mobility.[1,16] Given its similarity of honeycomb lattice to Gr and large bandgap (~6 eV), *h*-BN has become a promising material as a high-quality insulator and tunneling layer.[17,18] A plethora of reports have been communicated so far based on Gr and *h*-BN and shown many appealing properties.[9,18–20] For example, a room-temperature switching ratio of 50 has been obtained in the Gr/*h*-BN/Gr structure.[16]

However, tunneling devices based on vdWHs of Gr, *h*-BN, and TMDs have not been sufficiently studied despite the properties such as high mobility, high on/off ratio, and diverse band structure that emanate from TMDs.[21] Very recently, a metal–insulator–semiconductor (MIS) diode based on Gr/*h*-BN/MoS_2 was reported and showed good current rectification and high detectivity.[10,15] However, there still lacks detailed investigation of the tunneling behavior and the effect of *h*-BN thickness meant for improving the rectification ratio. More importantly, tunneling is strongly dependent on the band alignments, which has been demonstrated in Gr/*h*-BN/Gr vdWHs with different chemically doped Gr layers.[9] N-type $MoSe_2$ has smaller electron affinity than popular layered semiconductors (such as MoS_2 and black phosphorus),[21,22] which is expected to demonstrate higher tunneling performances. However, $MoSe_2$ has not been studied in this kind of heterostructure.

In this work, we report the fabrication of MIS vdWHs by vertically stacking Gr, *h*-BN, and n-type $MoSe_2$ using mechanical exfoliation and a dry transfer method. Their tunneling behavior was systematically studied. First, the tunneling nature was confirmed in a thin *h*-BN sandwiched device. On this basis, a large current modulation with the external electric field is demonstrated by sandwiching a thick *h*-BN layer, with a tunneling current on/off ratio of 5×10^3 and a current rectification ratio of 7×10^5. Furthermore, on account of this tunneling current, a non-volatile memory device with a high program/erase ratio, large memory window, and good retention characteristic is obtained.

The typical device structure and atomic schematic of the Gr/*h*-BN/$MoSe_2$ tunneling device are shown in Figures 1(a) and 1(b), respectively. Experimental details of the fabrication

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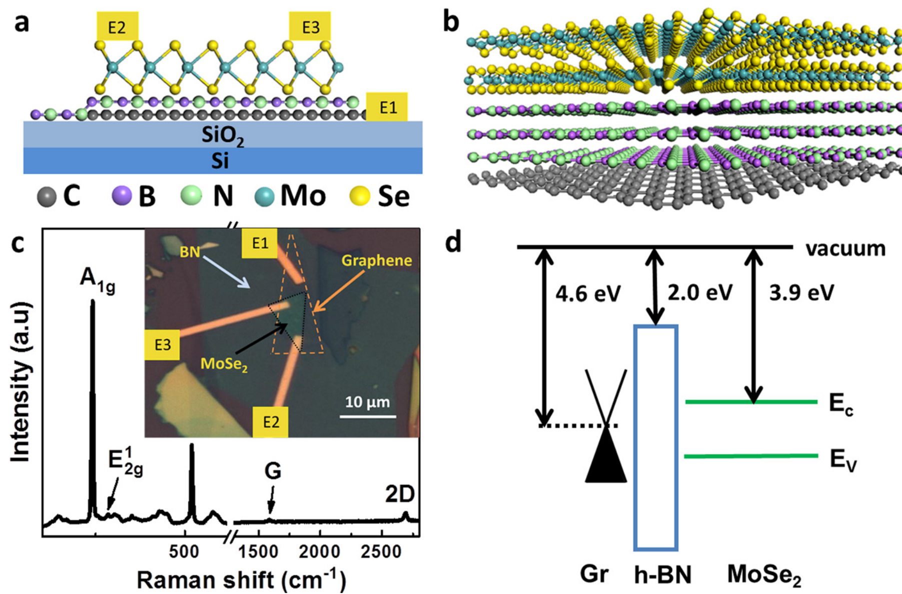

FIG. 1. Structure schematic (a) and atomic schematic (b) of the device with $MoSe_2$ on the top, *h*-BN in the middle, and graphene at the bottom. (c) Raman spectra of a typical device in the overlapped region. The inset is its corresponding optical image. The dotted lines indicate the boundaries of each 2D material. (d) Energy band diagrams of the device in the isolated state.

can be found in the supplementary material. It should be noted that E1 and E2 were used for the tunneling diode characterizations (E2 was kept grounded and E3 was suspended), while E2 and E3 were used for the memory characterizations (E3 was kept grounded and E1 was suspended). The degenerately doped silicon substrate is applied as a gate electrode. The inset of Figure 1(c) shows the optical microscopy (OM) image of our developed device (device 2). Its Raman spectra excited by the 532 nm laser are given in Figure 1(c). As can be seen, the strong A_{1g} and clear E_{2g}^{1} Raman modes of $MoSe_2$ are observed at 241 cm^{-1} and 285 cm^{-1}, indicating the existence of $MoSe_2$ in the device is in few-layer.[23,24] The Raman peaks at 1585 cm^{-1} and 2690 cm^{-1} are ascribed to the G and 2D modes of Gr. The high intensity ratio of I_{2D}/I_G (2.6) confirms its monolayer nature.[25] As for *h*-BN, its E_{2g} peak (1367 cm^{-1}) always associates with the disorder (D) peak of Gr around 1366 cm^{-1}, which makes it difficult to be identified.[26] The details of this part are given in Figure S3 in the supplementary material. The specific thickness of each layer was further confirmed by atomic force microscopy (AFM). The energy band diagram of the device in the isolated state is illustrated in Figure 1(d). The work function of Gr is about 4.6 eV.[10,12] The electron affinities of *h*-BN and few-layer $MoSe_2$ are 2–2.3 eV and 3.9–4.1 eV, respectively.[12,21] The bandgap of few-layer $MoSe_2$ is about 1.1 eV.[3] The transfer characteristic curve of $MoSe_2$ is given in Figure S4 in the supplementary material and exhibits obvious n-type conducting behavior. Considering the large potential difference between Gr and $MoSe_2$, superior rectification characteristic is expected.

Figure 2(a) shows the current versus voltage bias (I–V_b) curves, i.e., V_b was applied between Gr and $MoSe_2$, of our device (device 1) at 300 K and 80 K. The corresponding AFM image is given in Figure S2(a) in the supplementary material. The thickness of *h*-BN and $MoSe_2$ is identified to be 3.2 and 4.3 nm, respectively. It is obvious that there is no noticeable difference between two curves, demonstrating the tunneling-dominated transport. In addition, an asymmetric current with a rectification ratio of 3.75 is recorded. What is special here is the fact that under the positively biased condition, electrons can tunnel from $MoSe_2$ into Gr easily due to the decreased Fermi level of Gr and increased electron concentration of $MoSe_2$. On the contrary, it is difficult for electrons to pass through *h*-BN under a reverse bias due to the relatively higher barrier. As for the small amounts of holes at the valence band of $MoSe_2$, their direct tunneling is effectively blocked due to the high *h*-BN barrier. From the I–V_b curves under various gate voltages (V_g), as shown in Figure 2(b), it can be observed that the current can be modulated slightly. With a positive V_g, the Fermi level of Gr and $MoSe_2$ shifts upward, equivalent to reducing the barrier height for Gr (for reverse bias) and increasing the carrier concentration of $MoSe_2$ (forward bias). As a result, the current increases in both negative and positive bias regions. Conversely, a negative V_g would result in a decreased current. This phenomenon further solidifies the above discussed electron-dominated tunneling mechanism. Although it has shown a gate-tunable characteristic, tunneling current exhibits a weak dependence on V_g. We attribute this to the direct tunneling of carriers in the thin *h*-BN barrier, which may not be very sensitive to the barrier height compared with Fowler-Nordheim tunneling (FNT).[27] Had a thick *h*-BN flake been sandwiched, FNT is dominant, which may strongly depend on the barrier height. Therefore, tunneling current could be modulated easily by changing the Fermi level of graphene.

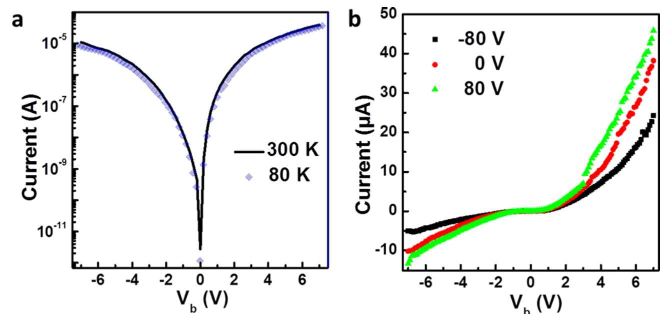

FIG. 2. (a) I–V_b curves of the tunneling device 1 on a logarithmic scale at 300 K and 80 K. (b) I–V_b curves of the tunneling device 1 under different gate voltages of −80 V, 0 V, and 80 V.

For the sake of experimentally evidencing this assumption, a thicker *h*-BN sandwiched device (device 2) was fabricated, as shown in Figure 1(c). The corresponding AFM image is given in Figure S2(b) in the supplementary material, from which the thickness of *h*-BN and $MoSe_2$ is determined to be 9.6 and 5.4 nm, respectively. Figure 3(a) shows its I–V_b curves under various V_g at room temperature. Unlike the case in the thinner one, an obvious off-state was observed at low bias. All output curves under different V_g, except −80 V, exhibit a sharp increase around ±5.6 V. The details of the off-state and sharp increase are given in Figure S5 in the supplementary material. This breakdown phenomenon is consistent with what have been observed in the Gr (metal)/*h*-BN/Gr structure.[9,17] With such relatively strong electrical field across *h*-BN, field-emission tunneling occurs. This tunneling behavior can be analyzed by the FNT formalism, namely, electrons go through the triangular barrier of *h*-BN. Its I–V_b characteristics follow equation:[17,27]

$$I(V_b) = \alpha A_{eff} V_b^2 \exp\left[-\frac{\beta}{V_b}\right], \tag{1}$$

where $\alpha = \frac{q^3 m_e}{8\pi h \Delta d^2 m^*}$ and $\beta = \frac{8\pi\sqrt{2m^*}\Delta^{\frac{3}{2}} \times d}{3hq}$.

Here, q is the electron charge, m_e is the free electron mass, h is the Planck constant, A_{eff} is the effective contact area of the stacked structure, and $m^* = 0.26\, m_e$,[28] Δ, and d are the effective electron mass, barrier height, and thickness of the *h*-BN layer, respectively. To better visualize this correlation, Equation (1) can be rearranged in a linear form

$$\ln\left(\frac{I}{V_b^2}\right) = \ln(\alpha A_{eff}) - \beta\frac{1}{V_b}. \tag{2}$$

Based on this FNT equation, $\ln(I/V^2)$ versus V^{-1} plots at high bias (both forward and reverse) are presented in Figure 3(b), using $V_g = 60$ V as an example (More conditions are given in Figure S6 in the supplementary material). A strong linearity was observed in the region $V_b > 5.8$ V and $V_b < -6.6$ V, suggesting the FNT-dominated transport. Besides, from the slope of fitted curve, the barrier height of *h*-BN can be extracted by

$$\Delta = \left(\frac{\beta \times 3hq}{8\pi\sqrt{2m} \times d}\right)^{\frac{2}{3}}. \tag{3}$$

Quantitatively, from the slope (−213) of the fitted curve in reverse bias, the calculated barrier height is 3.43 eV. This value is comparable to the previously reported value of 3.07 eV.[17] The slightly higher value can be attributed to different doped levels of Gr due to the impact of the substrate.[29] What is more, we further calculated the effective contact area and it is found to be 19.2 μm^2 from the intercept (−1.03) of the fitted curve, which is close to the measured value of the overlap (29 μm^2) from the corresponding OM image. Besides, tunneling current reaches 10^{-11} A at −7.5 V, where it can be defined as the breakdown voltage of the dielectric.[17] In view of the thickness of *h*-BN (9.6 nm), the calculated dielectric breakdown strength is 7.8 MV cm^{-1}, which agrees well with the previous report.[17] The above discussions confirm the tunneling nature of devices.

By utilizing this structure, large modulation of tunneling current is achieved. For a better illustration, the relevant band diagrams are displayed in Figure S8 in the supplementary material. With a large negative V_g (−80 V), a maximal potential difference between Gr and $MoSe_2$ is noticed,

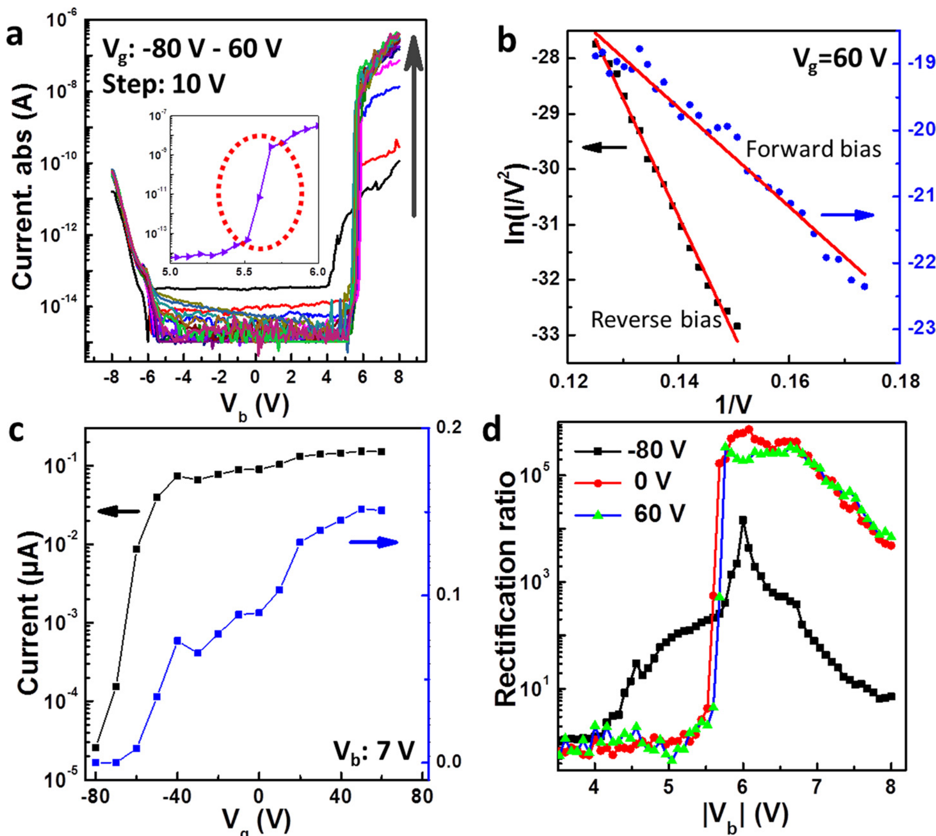

FIG. 3. (a) I–V_b curves of the tunneling device 2 on a logarithmic scale under different gate voltages from −80 V to 60 V (in 10 V steps). The inset is the detail of the sharp increase under zero gate voltage, as indicated by a red circle. (b) $\ln(I/V^2)$ vs. 1/V curves at high bias (both forward and reverse) for fitting of the Fowler-Nordheim tunneling model, using 60 V gate voltage as an example. Solid lines stand for the linear fit curves. (c) Current values of the device at a bias of 7 V under different gate voltages. (d) Rectification ratios of the device at bias from ±4 V to ±8 V under different gate voltages of −80 V, 0 V, and 60 V.

mainly reflected in the maximal off-state current aroused by direct tunneling. The current remains constant between bilateral breakdown voltages and increases at a smaller V_b in the forward region than other V_g. This phenomenon can be attributed to the extremely low Fermi level of Gr that can pull the barrier of *h*-BN into triangle severely. Consequently, FNT occurs with a small V_b. Besides, different from other curves, it is noteworthy that there is no sharp increase in the forward region under $V_g = -80\,V$ as a result of the depleted carrier concentration of $MoSe_2$. While increasing the V_g from $-70\,V$ to 60 V, the Fermi level of Gr increases, thus giving rise to the increasing carrier concentration of $MoSe_2$.[16,19,30] To quantitatively reveal the gate-controlled characteristic of the device, current values at a bias of 7 V under different V_g were extracted and are displayed in Figure 3(c). It can be clearly observed that the tunneling current in the forward region can be strongly modulated by V_g with an on/off ratio up to 5×10^3, exhibiting a typical tunneling field-effect transistor (FET) behavior. Different from the forward region, the current in the negative region shows a high consistence due to the strong screen effect of high reverse bias. As to the abrupt increase of current, it can be attributed to the accumulation of carriers at the interface. Generally, the thicker *h*-BN layer tends to accumulate more carriers at the interface between *h*-BN and $MoSe_2$ while less between graphene and *h*-BN. These accumulated carriers can pass through the *h*-BN layer in extremely short time during the breakdown. Thus with a thicker *h*-BN sandwiched, devices show a larger rectification ratio. With this asymmetric accumulation at the interface, a very large gate-controlled current rectification characteristic was obtained. Figure 3(d) shows the rectification ratios at bias from $\pm 4\,V$ to $\pm 8\,V$ under different V_g. A maximum rectification ratio of 7×10^5 was obtained at $\pm 6\,V$ under zero gate voltage. It is noteworthy that there is a small overlap between E2 and graphene, but we believe that it has little influence on the tunneling performance. The corresponding analysis is given in the supplementary material. The experiment results of other two devices are given in Figure S9 in the supplementary material and exhibit a similar phenomenon. To sum up, the devices show typical FET properties and an ultrahigh rectification ratio using a suitable *h*-BN layer.

Finally, based on the same device as shown in Figure 1(c) (device 2), 2D non-volatile memory was obtained. $MoSe_2$, *h*-BN, and Gr served as the channel, tunneling layer, and floating gate, respectively. A linear I_{sd}-V_{sd} characteristic of $MoSe_2$ is displayed in Figure S10 in the supplementary material, indicating a good ohmic contact. Figure 4(a) shows the transfer curve of the memory under different maximum gate voltages ($V_{g.max}$) at a bias of 0.05 V. A noticeable hysteresis can be observed along two different sweep directions of V_g, which is crucial for memory. Memory window, defined as the difference of threshold voltage during the dual-sweep of V_g, was extracted and is displayed in Figure 4(b). Memory window shows a strong dependence on $V_{g.max}$. The ratio of memory window and sweeping range can achieve 83.3% when $V_{g.max} = 90\,V$, which is the best recorded-value ever reported. Obviously, channel current has two distinct states, namely, program and erase. The relevant band diagrams to interpret this phenomenon are given in Figure 4(c). Through adding a positive V_g, electrons in the conduction band of $MoSe_2$ will tunnel into Gr and provide

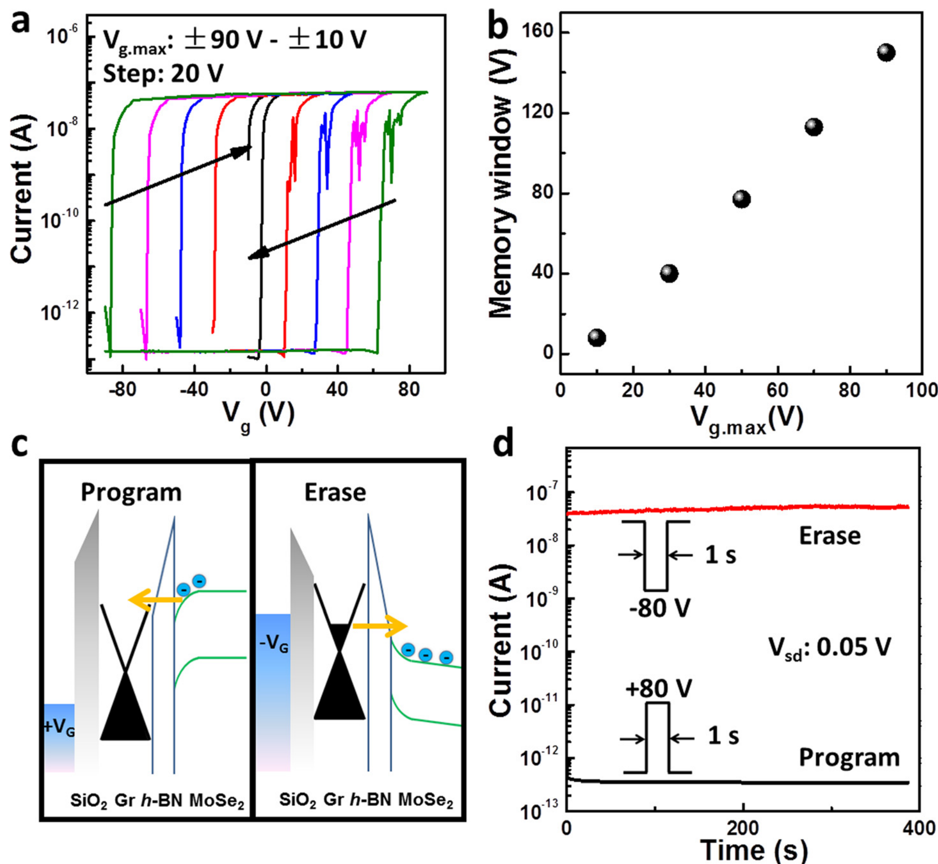

FIG. 4. (a) I–V_g curves of the memory under different maximum gate voltages from $\pm 90\,V$ to $\pm 10\,V$ (in 20 V steps) at $V_{sd} = 0.05\,V$. (b) The relationship between memory window and $V_{g.max}$. (c) Band diagram of the program/erase state of the memory under positive and negative gate voltage. (d) Retention characteristic of the memory.

sufficient gate-field screening, causing a positive shift of threshold voltage. Here, the memory is in the program state. When V_g becomes negative, the trapped electrons will be allowed to tunnel back to $MoSe_2$, thus causing a negative shift of threshold voltage. At this stage, the memory is in the erase state. To further demonstrate its retention characteristic, memory was programmed and erased to corresponding states through applying adverse voltage pulses ($V_g = \pm 80$ V, duration 1 s). The reading voltage was set as 0.05 V. A high program/erase (P/E) ratio exceeding 10^5 was maintained about 400 s, as displayed in Figure 4(d). This high P/E ratio makes it easy to read out the state of memory. Clear and stable switching behavior between program and erase states was also demonstrated, as shown in Figure S12 in the supplementary material.

In summary, we designed a multifunctional MIS vdWHs by vertically stacking Gr/*h*-BN/$MoSe_2$. Due to the relatively smaller electronic affinity of $MoSe_2$, device exhibits an ultra-high current rectification ratio, exceeding 7×10^5. The tunneling current can be strongly modulated by gate voltage with an on/off ratio up to 5×10^3, exhibiting a typical tunneling FET behavior. In addition, as a 2D non-volatile memory, it can achieve not only high program/erase ratio and large memory window but also good retention and switching characteristic. Therefore, this study could contribute to the fundamental understanding of tunneling behavior in vdWHs and pave the way for the integration based on 2DLMs.

See supplementary material for more experimental details and device characterizations.

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